SBC 86/87

TECHNICAL REFERENCE MANUAL

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Revision 1

April 1985

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CHAPTER 1 - INTRODUCTION TO THIS MANUAL

1.1 PURPOSE AND SCOPE

This manual was designed to explain everything you need to know to own, install, operate, evaluate, customize or write software for the Teletek SBC 86/87. This is a hardware manual only, and does not cover the use of any of the currently available software.

This manual is valid for Revision 1 boards.

1.2 ORGANIZATION

This manual provides the following chapters:

Chapter 1 explains how to use this manual, how it is organized, and other related documents that may be of interest to you.

Chapter 2 gives a general overview of the product and the intended application.

Chapter 3 explains how to install the board, including how to modify the hardware and how to connect peripherals.

Chapter 4 explains the logical operation of the board. This chapter presents the details of the hardware that a programmer would need to know to write either master or slave software.

Chapter 5 explains the hardware with more physical detail, including information that an electronic engineer would need to evaluate or test the product.

The manual ends with a specification summary and a board layout diagram.

1.3 RELATED DOCUMENTS

Some other documents may be of interest:

- Intel 8086, 8087, 8256, and 8259 Technical Manuals
- Signetics 2651 Technical Manual
- Customization and Application Notes

Intel and Signetics Technical Manuals present more complete information on the CPU and support chips than can be presented in this manual.

Customization Notes, which explain procedures not directly supported by the standard software, and Application Notes, which clarify existing information, may be available from Teletek from time to time.

CHAPTER 2 - INTRODUCTION TO THE SBC 86/87

The Teletek SBC 86/87 is a 16-bit slave single board computer intended for use on the IEEE-696/S-100 bus. This slave board is designed to communicate with an S-100 bus master via First-In-First-Out (FIFO) memory. Because the operation of this product is independent of the S-100 bus, several SBC 86/87s can be resident in a system at the same time, providing inexpensive multiple-processor, multiple-user system capabilities.

The features provided by the SBC 86/87 include:

* 16-bit 8086 CPU with optional 8087 Math Co-processor available in either 5 or 8 MHz
* 128K of RAM, with optional expansion to 512K
* 4K of EPROM, with optional expansion to 64K
* Two RS-232C compatible serial ports
* One Centronics compatible parallel port
* Five 8-bit counter/timer channels (four can be cascaded to two 16-bit counter/timers)
* On board interrupt controller
* Two independent FIFO buffers provided for S-100 data exchange

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CHAPTER 3 - HARDWARE INSTALLATION

3.1 STANDARD INSTALLATION PROCEDURE

A typical installation would require the following steps:

1. Inspect the SBC 86/87 for shipping damage.
2. Select the appropriate I/O address.
3. Make any option modifications.
4. Plug the board into the S-100 bus.
5. Attach the user console cable.
6. Attach any other local peripherals desired.
7. Boot the operating system disk.

3.2 VISUAL INSPECTION

Upon receipt of the SBC 86/87, check the shipping package for any signs of abuse while in transit. If you suspect that the package has been dropped or pierced, notify the shipping company immediately.

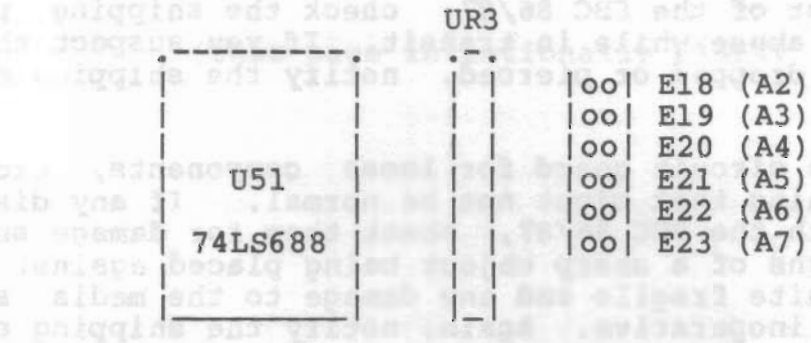
Inspect the circuit board for loose components, excessive moisture or anything that might not be normal. If any diskettes were shipped with the SBC 86/87, check them for damage such as bending, or signs of a sharp object being placed against them. Diskettes are quite fragile and any damage to the media surface will render them inoperative. Again, notify the shipping company if you find any damage.

3.3 I/O ADDRESSING

The SBC 86/87 occupies a cluster of four consecutive I/O ports, the base address of the cluster being a jumper selectable option. The option jumper plugs E18 through E23 corresponding to address lines A2 through A7, determine the address of the I/O cluster (see the diagram below). Where a jumper is in place, the corresponding address line will be seen as a zero (low). Where a jumper is out, the address line will be seen as a one (high).

Remember, the address jumpers determine the base I/O port address for each individual SBC 86/87 board. The four consecutive port addresses in the cluster are decoded by on-board logic. The address jumpers allow the choice of any base address within the I/O address range of 00 through FC hex.

These jumpers are located in the lower center of the board, to the right of U51. See "Appendix B - Board Layout Diagram".



EXAMPLE: To configure the SBC 86/87 for a base I/O address of 40 hex (which includes the cluster of addresses 40-43 hex) arrange the jumpers in the following manner:

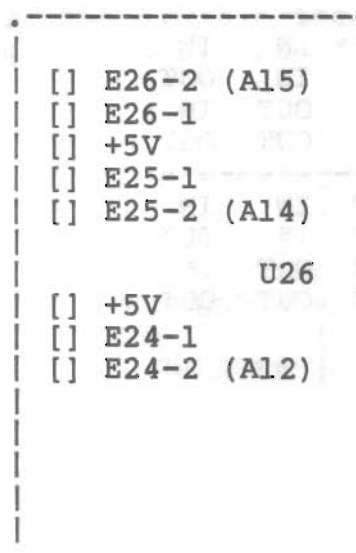
E18	IN
E19	IN
E20	IN
E21	IN
E22	OUT
E23	IN

The following table illustrates the jumper configurations for base I/O addresses in the range from 40 to 7C hex.

I/O Address	E23 A7	E22 A6	E21 A5	E20 A4	E19 A3	E18 A2
40-43	IN	OUT	IN	IN	IN	IN
44-47	IN	OUT	IN	IN	IN	OUT
48-4B	IN	OUT	IN	IN	OUT	IN
4C-4F	IN	OUT	IN	IN	OUT	OUT
50-53	IN	OUT	IN	OUT	IN	IN
54-57	IN	OUT	IN	OUT	IN	OUT
58-5B	IN	OUT	IN	OUT	OUT	IN
5B-5F	IN	OUT	IN	OUT	OUT	OUT
60-63	IN	OUT	OUT	IN	IN	IN
64-67	IN	OUT	OUT	IN	IN	OUT
68-6B	IN	OUT	OUT	IN	OUT	IN
6C-6F	IN	OUT	OUT	IN	OUT	OUT
70-73	IN	OUT	OUT	OUT	IN	IN
74-77	IN	OUT	OUT	OUT	IN	OUT
78-7B	IN	OUT	OUT	OUT	OUT	IN
7C-7F	IN	OUT	OUT	OUT	OUT	OUT

3.4 ROM OPTIONS

The SBC 86/87 can support two 2716, 2732, 2764, 27128, or 27256 EPROMs (2K, 4K, 8K, 16K and 32K bytes, respectively) as well as their masked-ROM counterparts. U26 provides the data bits D0-D7 (the low or even byte), while U27 provides data bits D8-D15 (the high or odd byte). The standard product is set up for the 2716 (2K) EPROM. If a different size is desired, traces can be cut and jumper wires added behind U26 to support the desired device. The tables below summarize the requirements. In each case, cut the trace already leading from the indicated pin, and replace it with a jumper wire from the pin to the indicated "E" pad. The "E" pads are labeled on the solder side of the board.



EPROM	CONNECT:
2716	E26-1 to +5V E25-1 to +5V E24-1 to +5V
2732 or 2764	E26-1 to +5V E25-1 to +5V E24-1 to E24-2
27128	E26-1 to +5V E25-1 to E25-2 E24-1 to E24-2
27256	E26-1 to E26-2 E25-1 to E25-2 E24-1 to E24-2

3.5 PERIPHERAL CONNECTIONS

For both serial ports, the peripheral connections need only be flat ribbon cables with the appropriate 16-pin crimp style connectors. The pin-out of the serial port connector corresponds to the first 16 lines of the DB-25 connector used for RS-232-C communications. Therefore, by aligning pin 1 of the female plug with pin 1 of the DB-25 connector, a length of 16 conductor flat ribbon cable can be used to make the cable.

For the parallel port a custom cable is required from Teletek (order TEI part number D1050) that will adapt the 10-pin connector on the SBC 86/87 to the Centronics compatible 36-pin connector.

The location of each of the cable connectors is shown in "Appendix B - Board Layout Diagram". Connectors J-1 and J-2 are connected to serial ports A and B respectively. Connector J-3 is connected to the parallel port. All these male connectors are keyed to allow the use of similarly keyed female connectors. If keyed female connectors are not used, make sure that pin 1 of each cable is toward the left edge of the board when the cable is installed.

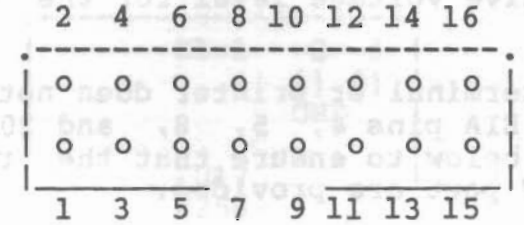
Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable, as this may cause the cable to separate from its crimp connection and cause intermittent problems.

It is possible to order pre-assembled cables meeting your specifications directly from Teletek. Contact Teletek for pricing and shipping information.

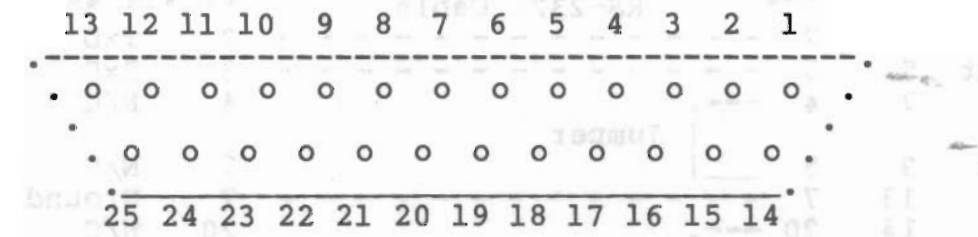
3.5.1 Serial Terminal or Printer Configuration

In this standard configuration, each serial channel appears as EIA Data Communication Equipment (DCE), and will connect directly to a terminal or a printer. The connectors on the SBC 86/87 have the following pin assignments:

J1 & J2



EIA RS-232C
DB-25 FEMALE CONNECTOR



Either channel can be crimp-connected to a 25-pin RS-232-C connector by aligning pin 1 of the cable from the SBC 86/87 16-pin connector with pin 1 of the 25-pin RS-232-C connector.

Serial port A (J1) is provided by the 2651 USART and expects the full RS-232C handshaking as shown below:

SBC 86/87 USART Signal	J1 Pin	DB-25 Pin	RS-232C Cable	Terminal/Printer EIA Pin	Terminal/Printer EIA Signal
Data In	3	2	- - - - - - - - - - - - - - - -	2	TxD
Data Out	5	3	- - - - - - - - - - - - - - - -	3	RxD
DCD In	7	4	- - - - - - - - - - - - - - - -	4	RTS
DTR Out	9	5	- - - - - - - - - - - - - - - -	5	CTS
Ground	13	7	- - - - - - - - - - - - - - - -	7	Ground
CTS In	14	20	- - - - - - - - - - - - - - - -	20	DTR
RTS Out	15	8	- - - - - - - - - - - - - - - -	8	DCD

"In" and "Out" refer to the direction of the signal with respect to the SBC 86/87. Signals from the peripheral device are IN to the SBC 86/87. Signals to the peripheral device are OUT.

The EIA signals CTS (Clear To Send) and DCD (Data Carrier Detect) are outputs to the external device and are at a positive voltage levels when the USART channel is ready to function. RTS (Request To Send) and DTR (Data Terminal Ready) are inputs which must be at a positive voltage level for the USART channel to function.

Note: If the terminal or printer does not provide RTS, CTS, DCD, and DTR then EIA pins 4, 5, 8, and 20 must be jumpered together as shown below to ensure that the required handshake signals to the USART port are provided:

SBC 86/87 USART Signal	J1 Pin	DB-25 Pin	RS-232C Cable	Terminal/Printer DB-25 Pin	Terminal/Printer DB-25 Signal
Data In	3	2	- - - - - - - - - - - - - - - -	2	TxD
Data Out	5	3	- - - - - - - - - - - - - - - -	3	RxD
DCD In	7	4	---.	4	N/C
			| Jumper		
DTR Out	9	5	___|	5	N/C
Ground	13	7	- - - - - - - - - - - - - - - -	7	Ground
CTS In	14	20	---.	20	N/C
			| Jumper		
RTS Out	15	8	___|	8	N/C

Serial port B (J2) is provided by the 8256 MUART. The MUART provides only one hardware handsake line (CTS In), the other handshake signals are generated by using software controlled bits from parallel port 1. The output control EIA signals DCD and CTS are set active during initialization and always remain active during normal operation. Software drivers may be written to provide full RS-232C handshake compatibility if your application requires this feature.

SBC 86/87 MUART Signal	J2 Pin	DB-25 Pin	RS-232C Cable	Terminal/Printer DB-25 Pin	Signal
Data In	3	2	- -	2	TxD
Data Out	5	3	- -	3	RxD
P14 In	7	4	- -	4	RTS
P16 Out	9	5	- -	5	CTS
Ground	13	7	- -	7	Ground
CTS In	14	20	- -	20	DTR
P15 Out	15	8	- -	8	DCD

The option jumper E1 enables the MUART CTS signal to be connected to EIA pin 20 (DTR). Normally this input is connected to ground (E1-1 to E1-2) always enabling the transmitter. To enable this feature jumper E1-3 to E1-1.

3.5.2 Modem Configuration

If the USART channel is to connect to a modem, which is always EIA Data Communication Equipment (DCE), that channel must appear as EIA Data Terminal Equipment (DTE). All the configuration details are the same as for a terminal or printer, except that six of the seven RS-232-C connections must be moved to the appropriate lines from the modem. The connections should be as follows:

SBC 86/87 USART Signal	J1 Pin	DB-25 Pin	RS-232C Cable	Modem EIA Pin	Modem Signal
Data In	3	2	- - - - - - - - - - - - - - - - - - -	3	RxD
Data Out	5	3	- - - - - - - - - - - - - - - - - - -	2	TxD
DCD In	7	4	- - - - - - - - - - - - - - - - - - -	8	DCD
DTR Out	9	5	- - - - - - - - - - - - - - - - - - -	20	DTR
Ground	13	7	- - - - - - - - - - - - - - - - - - -	7	Ground
CTS In	14	20	- - - - - - - - - - - - - - - - - - -	5	CTS
RTS Out	15	8	- - - - - - - - - - - - - - - - - - -	4	RTS

"In" and "Out" refer to the direction of the signal with respect to the SBC 86/87. Data and signals from the modem are IN to the SBC 86/87, while data and signals to the modem are OUT.

3.5.3 Baud Rate Selection

Baud rates for both serial ports on the SBC 86/87 are under software control and can be changed by altering the appropriate I/O registers within the 2651 UART or the 8256 MUART. Normally these registers are set during initialization to default values chosen by the operating system.

3.5.4 Parallel Port Configuration

The parallel port (J3) provided by the MUART will support one Centronics compatible printer. The port is capable of sending 7-bit ASCII data to the printer in two modes. The standard mode which is compatible with most printers utilizes the automatic hardware handshake of the MUART and will generate an interrupt upon receipt of the /ACK signal from the printer.

The optional mode available utilizes a software controlled strobe enable (P13) that will work with printers that are not compatible with the MUART hardware protocol. The connections for an adapter cable should be as follows:

SBC 86/87 MUART Signal	J3 Pin	Cable	Centronics 36 Pin Connector Pin	Signal
P11*P13	1	- - - - - - - - - - - - - - - -	1	/STB
P20	2	- - - - - - - - - - - - - - - -	2	D1
P21	3	- - - - - - - - - - - - - - - -	3	D2
P22	4	- - - - - - - - - - - - - - - -	4	D3
P23	5	- - - - - - - - - - - - - - - -	5	D4
P24	6	- - - - - - - - - - - - - - - -	6	D5
P25	7	- - - - - - - - - - - - - - - -	7	D6
P26	8	- - - - - - - - - - - - - - - -	8	D7
GND	9	- - - - - - - - - - - - - - - -	9 16	D8 & GND
P10	10	- - - - - - - - - - - - - - - -	10	/ACK

3.6 COOLING

The SBC 86/87 needs to be in a well ventilated area due to the high density of ICs on the board. Ideally, the board should be mounted vertically in a stream of air which will be moving across its face. Also, ensuring that the fan is close to the card cage will provide the optimum cooling. Whatever the position, forced air cooling is mandatory.

3.7 IN CASE OF TROUBLE

If the SBC 86/87 does not respond the first time it's connected, relax. Take the time to read the manual thoroughly, especially the "Peripheral Connections" section. The following trouble-shooting guide lists the most common problems.

1. Check the console cable and verify the handshaking signals. Make sure the console is set at the proper baud rate.

2. Communications between the SBC 86/87 and the system may be somehow impaired. Have the correct options/modifications been added to the board for the operating system being used? Has the operating system been correctly configured for the SBC 86/87? Is the SBC 86/87 I/O port addressing correct both on the board and in the operating system?

3. If the console and cable are working properly, the correct hardware option modifications have been added, and the operating system has been correctly configured, the SBC 86/87 itself may be faulty. Does the on-board monitor firmware come up? If the monitor is working the board is probably functional and you can use the monitor to debug the system interface. If not try another SBC 86/87 if one is available. Otherwise return the board to Teletek for check-out.

CHAPTER 4 - LOGICAL HARDWARE OPERATION

This chapter explains those details of the hardware that a programmer would need to know to write master or slave software. First the operation of the SBC 86/87 from the master's point of view is presented. Then the view from inside one slave is described. Finally, information on communication between the two is given.

4.1 EXTERNAL VIEW

This section explains the logical operation of the SBC 86/87 as seen from the outside, such as by software running on the master.

4.1.1 Port Assignments

The SBC 86/87 occupies a cluster of four consecutive I/O ports. The functions of each port are as follows:

port0	input =	read from slave status register
	output =	send Tx INT to slave, reset TxRDY flag to master
port1	input =	read data from slave TxFIFO
	output =	write data to slave RxFIFO
port2	input =	send Aux INT to slave, reset Aux flag to master
	output =	reset slave RxFIFO address counters
port3	input =	reset the slave
	output =	send Rx INT to slave, reset RxRDY flag to master

The actual I/O address of the port cluster depends on four hardware option jumpers. See the "Hardware Options" section of this manual for information on setting or changing the port addresses.

4.1.2 Reset

There are two levels of reset available on the SBC 86/87. The first is a system reset in which all boards (and therefore all users) in the system are reset simultaneously by activating the /RESET signal (pin 75) on the S-100 bus. The second type of reset is done through software. The master writes to the "reset the slave" S-100 I/O port to individually reset one slave. This allows the master CPU to "wake up" a user that doesn't respond to an inquiry.

4.1.3 Interrupts

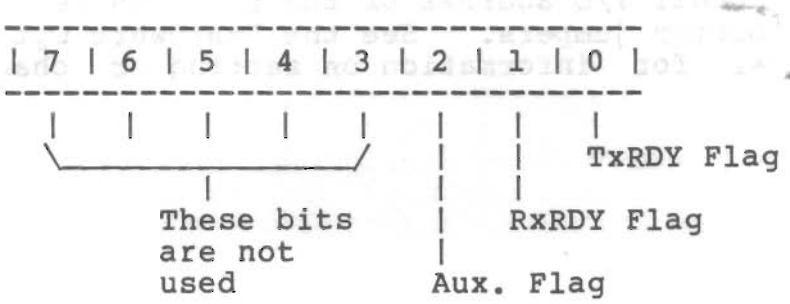
The bus master can cause three different interrupts to the slave: the Rx INT, the Tx INT, and the Aux INT. Any time one of these interrupts is sent to the slave by accessing the appropriate I/O port, the associated flag in the status register is cleared.

The Rx INT is used to indicate to the slave that the master has written data to the slave RxFIFO. The Tx INT is used to indicate that data has been read by the master from the slave TxFIFO. The Aux INT and Aux flag in the status register are free for programmer defined functions, the most common usage being for a "slave running" check where the master sends an Aux INT to the slave and the slave responds by setting the Aux flag in the status register.

4.1.4 Status Register

The status register contains three flags that can be set by the slave and read or cleared (by sending interrupts) by the master. This register is normally polled by the master during network communications over the S100 bus. The following diagram illustrates how this register is defined:

Slave to Master Status Register Bits



4.2 INTERNAL VIEW

This section explains the logical operation of the SBC 86/87 as seen from the inside. This is what the world looks like to software running on one slave.

4.2.1 Port Assignments

The functions of each on-board I/O port are as follows:

Hex Address	Read Function	Write Function	
00	Command 1	Command 1	
02	Command 2	Command 2	
04	Command 3	Command 3	
06	Mode	Mode	
08	Port 1 Control	Port 1 Control	
0A	Interrupt Enable	Set Interrupts	
0C	Interrupt Address	Reset Interrupts	
0E	Receiver Buffer	Transmitter Buffer	(8256
10	Port 1	Portl	MUART)
12	Port 2	Port2	
14	Timer 1	Timer 1	
16	Timer 2	Timer 2	
18	Timer 3	Timer 3	
1A	Timer 4	Timer 4	
1C	Timer 5	Timer 5	
1E	Status	Modification	
20	Receiver Buffer	NA	
22	Status	NA	(2651
24	Mode	NA	USART)
26	Command	NA	
28	NA	Transmitter Buffer	
2A	NA	SYN1/SYN2/DLE	
2C	NA	Mode	
2E	NA	Command	
30	8259 PIC (A0 = 0)		
32	8259 PIC (A0 = 1)		
40	Clear + Enable PEI	Clear TFIFO Address	
42	Clear Tx INT	Set TxRDY Flag to master	
44	Clear Rx INT	Set RxRDY Flag to master	
46	Clear Aux. INT	Set Aux. Flag to master	
50	Read RxFIFO	Write TxFIFO	
60	NA	Disable PEI	

4.2.2 Interrupts

The SBC 86/87 supplies two cascaded eight level Priority Interrupt Controllers (PICs) to resolve all interrupts from on-board and from the system master. An Intel 8259A acts as the master PIC with the second PIC provided by an Intel 8256 MUART. The following tables show the PIC assignments as well as the Non-Maskable Interrupt (NMI) assignment:

8259A PIC

Number	Usage
NMI	Memory Parity Error
0	MUART
1	USART Transmit Buffer Empty
2	USART Receive Data Available
3	Tx INT from master
4	Rx INT from master
5	Aux. INT from master
6	8087 NPX
7	EXPANSION BUS

8256 MUART

Number	Usage
0	Timer 1
1	Timer 2 or Port 1 P17 Interrupt
2	External Interrupt (EXTINT)
3	Timer 3 or Timers 3 & 5
4	Receiver Interrupt
5	Transmitter Interrupt
6	Timer 4 or Timers 2 & 4
7	Timer 5 or Port 2 Handshaking

The slave must clear any interrupt from the master before the master can set that interrupt again. This is done by reading the appropriate on-board I/O port during the interrupt service routine for that interrupt.

The NMI parity interrupt is normally enabled but can be disabled by writing to I/O port 060 hex (Disable PEI). To clear a parity error and enable the NMI read I/O port 040 hex (Enable PEI).

4.2.3 Reset Sequence and ROM Control

After a reset operation, the CPU begins fetching instructions from FFFF0 hex, where the on-board EPROM/ROM resides. The firmware immediately jumps to the beginning of the EPROM/ROM space at F0000 hex and begins initialization of the on-board devices. This ROM occupies location F0000h to FFFFFh, a 64K word block, and is enabled at all times.

Note that depending on the size of the particular EPROM device installed, it may be that not all 64K words of the ROM block actually contains ROM. In cases where the EPROM is smaller than the available space, the firmware will repeat itself on boundaries the same size as the device in use.

4.2.4 Character I/O and Clock

The SBC 86/87 provides two ports for serial communication, one from an Intel 8256 MUART and the other from a Signetics 2651 USART. In addition the MUART also provides the timer/counter channels and the Centronics compatible parallel port. Information on programming these chips is beyond the scope of this document, but is presented in the Microsystem Components Handbook available from Intel and the MOS Microprocessor Data Manual available from Signetics.

4.3 MASTER / SLAVE COMMUNICATION

This section explains the logical operation of communication details visible from both the master and the slave.

4.3.1 Data Exchange

All information exchanged between the S-100 bus master and a the SBC 86/87, other than protocol control signals, occurs via the dual FIFO memory circuit on board the slave. This circuit is based on a byte-wide static RAM device. Each time a byte is read from or written to the FIFO, a counter circuit automatically increments the address lines. This counter can be reset to the beginning address by either the master or the slave (depending upon which FIFO), by accessing their respective "clear FIFO address counters" I/O ports.

4.3.2 General Protocol

The recommended network interface is as follows:

Slave Operations -

```
SLAVE SEND
     Wait for TxFIFO available
     Reset TxFIFO address counters
     Transfer data to TxFIFO
     Reset TxFIFO address counters
     Set TxRDY flag to master

SLAVE SEND ACKNOWLEDGE/INTERRUPT
     Clear Tx INT
     Signal TxFIFO available

SLAVE RECEIVE
     Wait for RxFIFO full
     Transfer data from RxFIFO
     Set RxRDY flag to master

SLAVE RECEIVE ACKNOWLEDGE/INTERRUPT
     Clear Rx INT
     Signal RxFIFO full

Semaphore TxFIFO available initialized to available
Semaphore RxFIFO initialized to empty
Semaphore TxRDY initialized to not ready
Semaphore RxRDY initialized to ready
```

Master Operations -

```
MASTER SEND
     Poll-wait for RxRDY to be set
     Reset RxFIFO address counters
     Transfer data to RxFIFO
     Reset RxFIFO address counters
     Send Rx INT to slave (reset RxRDY)

MASTER RECEIVE
     Poll-wait for TxRDY to be set
     Transfer data from TxFIFO
     Send Tx INT to slave (reset TxRDY)
```

The Aux status bit and interrupt normally is used for a "slave running" check as follows:

```
MASTER
     Send Aux INT to slave (reset Aux flag)
     Poll-wait for Aux flag set or timeout

SLAVE ACKNOWLEDGE/INTERRUPT
     Clear Aux INT
     Set Aux flag to master
```

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CHAPTER 5 - PHYSICAL HARDWARE OPERATION

This chapter explains those details of the hardware that an electronic engineer would need to evaluate or test the SBC 86/87.

5.1 CENTRAL PROCESSOR

The SBC 86/87 utilizes the Intel 8086 CPU, at either 5 or 8 MHz, and peripheral support chips from both Intel and Signetics. Since the SBC 86/87 operates independently of the S-100 bus, the internal speed of operation can be different from that of the main system CPU.

The SBC 86/87 also provides an optional 8087 numeric data coprocessor. This coprocessor adds arithmetic, trigonometric, exponential, and logarithmic instructions to the standard 8086 instruction set. The 8087 will significantly improve the performance of the CPU during numeric intensive operations. The 8087 coprocessor conforms to the proposed IEEE Floating Point Standard.

5.2 MEMORY

The standard SBC 86/87 provides 128K bytes of RAM, expandable to 512K by using 256K-bit RAM ICs. The standard board uses stacked RAM ICs to reduce the physical size of the array. The board also provides 4K bytes of EPROM standard using two 2716s, and is expandable to 64K bytes by using two 27256 EPROMs.

The on-board RAM controller that supports either 64K or 256K devices is an Intel 8208. It provides the necessary signals to address, refresh, and directly drive the memory array. The controller is automatically initialized upon reset by a 74LS165 shift register.

No CPU wait states are used or required when accessing RAM memory on either the 5 or 8MHz products. A single wait state is inserted for each access of the EPROM or ROM. This cannot be altered by the user.

5.3 CLOCK GENERATION

The SBC 86/87 utilizes the Intel 8284A clock generator and driver to provide the system and peripheral clocks. This IC also synchronizes the CPU READY function and generates the RESET ouput to the CPU and support chips.

5.4 I/O SELECT LOGIC

Decoding and selection of on-board I/O functions is handled by components U14 and U18, a 74LS155 and a custom programmed PAL. These circuits decode address lines A1 through A7 to form the necessary chip select signals, register select signals, and other control signals.

5.5 SERIAL I/O

The SBC 86/87 provides two ports for serial communication, one from the 8256 MUART and the other from a Signetics 2651. Only the details that are unique to the SBC 86/87 are presented in this section. Complete technical information on these chips is beyond the scope of this document, but is presented in the Microsystem Components Handbook available from Intel and the MOS Microprocessor Data Manual available from Signetics.

5.5.1 EIA Serial Data Transfer Protocol

Prior to sending or receiving data, the four handshake lines should be active low. However, the 2651 USART will allow control of its receive and transmit functions independently. If the hardware hankshake functions of the USART are enabled (standard), the 2651 will not send data until CTS is low. This is handy for buffered printers which need to stop receiving data until the buffer is printed. By pulling CTS high, the printer will stop the flow of data from the USART. When it is ready to receive more data, it pulls CTS low. Similarly, the 2651 will not accept information until DCD is low. This is primarily used with a communications link, where, if signal conditions deteriorate, the data may be garbled.

5.5.2 RS-232-C Voltage Levels

A logic high (a binary one), or marking condition, is any voltage between -3 volts and -25 volts. A logic low (a binary zero), or spacing condition, is any voltage between +3 volts and +25 volts. Any level between -3 and +3 volts is undefined. This is called the transition region. The maximum transition time between bit cells is four percent of the basic clock period. The maximum voltage rate of change (slew rate) is 30 volts/uSec. The maximum RS-232-C transmission speed is 20,000 baud.

5.5.3 Serial Data Timing

Prior to transmitting data, the signal line is held high (marking). It goes low (spacing) to indicate the start of a character. The bits representing the character are sent least significant bit first, then a parity bit (if used), and finally two stop bits. The stop bits indicate the end of the character and are always logic high. The standard SBC 86/87 is set up for eight data bits, no parity, and two stop bits.

The value of each character bit is held for the entire length of each bit cell. The length in time of each bit cell is the basic clock period, equal to the reciprocal of the baud rate. For example, at 9600 baud the length of each bit cell is:

$$\frac{1}{9600 \text{ cycles/second}} = .0001041 \text{ seconds} = 104.1 \text{ microseconds}$$

5.6 PARALLEL I/O

One Centronics compatible parallel port is provided by the Intel 8256 MUART. This interface provides seven data lines, the /STB control line, and the /ACK control line. Handshake timing is controlled by the 8256 automatically. An optional protocol allows the use of a software controlled strobe (P13 of the MUART) to enable the /STB signal to the printer. This allows a slower driver to be utilized that will work for printers that are not compatible with the MUART hardware handshake timing. The parallel interface also provides the line drivers required for longer cables and eliminates the need for external paddle boards.

5.7 COUNTER/TIMERS

The counter/timer functions are also provided by the Intel 8256 MUART. Five 8-bit programmable channels are supplied, and these can be cascaded to form two 16-bit channels if desired. The clock source for these circuits comes from the 5.0688 MHz oscillator used with the 2651 USART.

5.8 INTERRUPTS

The Intel 8259 programmable interrupt controller provides up to eight priority levels of interrupts, allowing efficient operation of the on-board I/O devices as well as optimizing the master-slave FIFO protocol.

5.9 S-100 INTERFACE

The SBC 86/87 cannot function as the bus master of a system, and therefore depends on a master system processor to manage all of the system data transfers through the 2K FIFOs. The FIFOs appear to be I/O ports to the master.

This method of system communication combines the simplicity of mapping the slaves as ports in the master I/O space with the high performance provided by using block data transfers between the master and slave boards. Unlike a traditional DMA based system, master and slave processors do not both have to be idle during the transfer. Using the FIFO method, the slave processor is free to perform normal operations during the time that the data transfers are taking place between the master processor and the FIFO. Another advantage is that both the master and slave processor are free to answer interrupt requests at any time during the transfer.

Asynchronous communication is inherent in the design of this type of system. The master processor and slave SBC 86/87s in the system are operating independently of each other. In fact the master processor and the SBC 86/87s can be running at completely different clock speeds altogether. This capability allows the system designer to place high speed processing power where it is needed in the system and use low cost standard speed CPUs for the remaining system functions.

There are two levels of reset available on the SBC 86/87. The first is a system reset in which all boards (and therefore all users) in the system are reset simultaneously by activating the RESET* signal (pin 75) on the S-100 bus. The second type of reset is a software reset where the master issues an I/O command to idividually reset one user. This allows the master CPU to "wake up" a user that doesn't respond to an inquiry.

The SBC 86/87 is fully IEEE-696 (S-100) compatible and supports all I/O operations which might be implemented in an I/O port accessed device.

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APPENDIX A -- SPECIFICATIONS

CPU

8086, 5 MHz standard, 8 MHz optional.
Optional 8087 Math Coprocessor.

MEMORY

EPROM: Two 2716, 2732, 2764, 27128, or 27256 devices may be used. 2716 is standard.

FIFO: Two 2K byte static RAMs.

RAM: 128K bytes using 64K-bit RAM ICs standard. 512K bytes using 256K-bit RAM ICs optional. Uses 200ns dynamic RAM at 5 MHz, and 150ns dynamic RAM at 8 MHz.

HOST INTERFACE

Occupies four consecutive I/O ports. Address of base port is selected with jumpers, and must be on a 4-port boundary.

SBC 86/87 uses the following S-100 signals:

Pin	Signal	Use
45	sOUT	Output Status Signal
46	sINP	Input Status Signal
75	/RESET	System Reset
77	/pWR	Write Strobe
78	pDBIN	Read Strobe
	A0-A7	Address Lines
	DO0-DO7	Data Out Lines
	DI0-DI7	Data In Lines
	+8 Volts @ 2.5A	
	+16 Volts @ 50mA	
	-16 Volts @ 50mA	
	GND	

PERIPHERAL INTERFACE

Two independent RS-232C serial ports. Software selectable speeds from 300 to 19200 baud. One Centronics compatible parallel port.

COOLING

Forced air cooling required.

DIMENSIONS

5.125" x 10.00", excluding edge connector.

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APPENDIX B -- BOARD LAYOUT DIAGRAM